# PHYSICS 1 – SYGS – SEM IV

## PRACTICE TEST QUESTION

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| **1** | Fresnel's diffraction due to a narrow wire; the fringe width _____ if the diameter of the wire increased.<br>a) remains same<br>b) decreases<br>c) increases<br>d) reduces to zero |
| **2** | According to Huygens's theory; "No back wave" only forward propagation of a wavefront is effective then for 'obliquity factor ' θ is _____<br>a) 0°<br>b) 90°<br>c) 180°<br>d) reduces to zero |
| **3** | Diffraction effect can be observed in _____<br>a) only sound waves<br>b) only light waves<br>c) only ultra-sonic wave<br>d) sound and light waves both |
| **4** | Direction of first secondary maximum in the Fraunhofer diffraction pattern at a single slit is given by (a = width of the slit) _____.<br>a) a sinθ= λ/2<br>b) a cosθ= 3λ/2<br>c) a sinθ= λ<br>d) a sinθ= 3λ/2 |
| **5** | The angle between pass axis of polarization and analyser is 45° . The percentage of polarized light passing through analyser is _____<br>a) 75%<br>b) 25%<br>c) 100%<br>d) 50% |
| **6** | Transverse nature of light was confirmed by the phenomenon of _____ of light.<br>a) Refraction<br>b) Diffraction<br>c) Dispersion<br>d) polarization |
| **7** | In the case of linearly polarized light , the magnitude of the electric field vector_____<br>a) Is parallel to the direction of propagation<br>b) does not change with time |

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| | c) increases linearly with time<br>d) varies periodically with time |
| **8** | Which of the following is a uniaxial crystal?<br>a) Borax<br>b) Mica<br>c) Quartz<br>d) Selenite |
| **9** | The number of nibbles, which make up one byte is _____<br>a) 2<br>b) 4<br>c) 6<br>d) 12 |
| **10** | A full adder consists of _____<br>a) AND gate<br>b) NAND gate<br>c) EXOR and AND gate<br>d) EXOR and OR gate |
| **11** | Flipflops can be used to store _____<br>a) one byte data<br>b) one bit data<br>c) two bit data<br>d) two byte data |
| **12** | Any sequential logic circuit consists of _____<br>a) only flip flops<br>b) only logic gates<br>c) flip flops and logic gates<br>d) only combinational logic gates. |
| **13** | $(4DCB)_{16} = ( ? )_8 = ( ? )_{10}$<br>a) $(46713)_8$ and $(19915)_{10}$<br>b) $(467)_8$ and $(19915)_{10}$<br>c) $(46713)_8$ and $(115)_{10}$<br>d) $(48713)_8$ and $(29915)_{10}$ |
| **14** | Half-adders have a major limitation in that they cannot _____<br>a) Accept a carry bit from a present stage<br>b) Accept a carry bit from a next stage<br>c) Accept a carry bit from a previous stage<br>d) Accept a carry bit from the following stages |
| **15** | How many AND, OR and EXOR gates are required for the configuration of full adder?<br>a) 1, 2, 2<br>b) 2, 1, 2<br>c) 3, 1, 2<br>d) 4, 0, 1 |